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UWB Design Issues and How the  
*New* SPW Can Help You be  
Successful

December 2003

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# Agenda

- Introductions
- Wireless Industry – Design Issues  
Dr. Heinrich Meyr
- Opportunities for UWB Design  
Dr. Rafie
- CoWare / SPW Update  
Eshel Haritan
- Live, Interactive Q&A

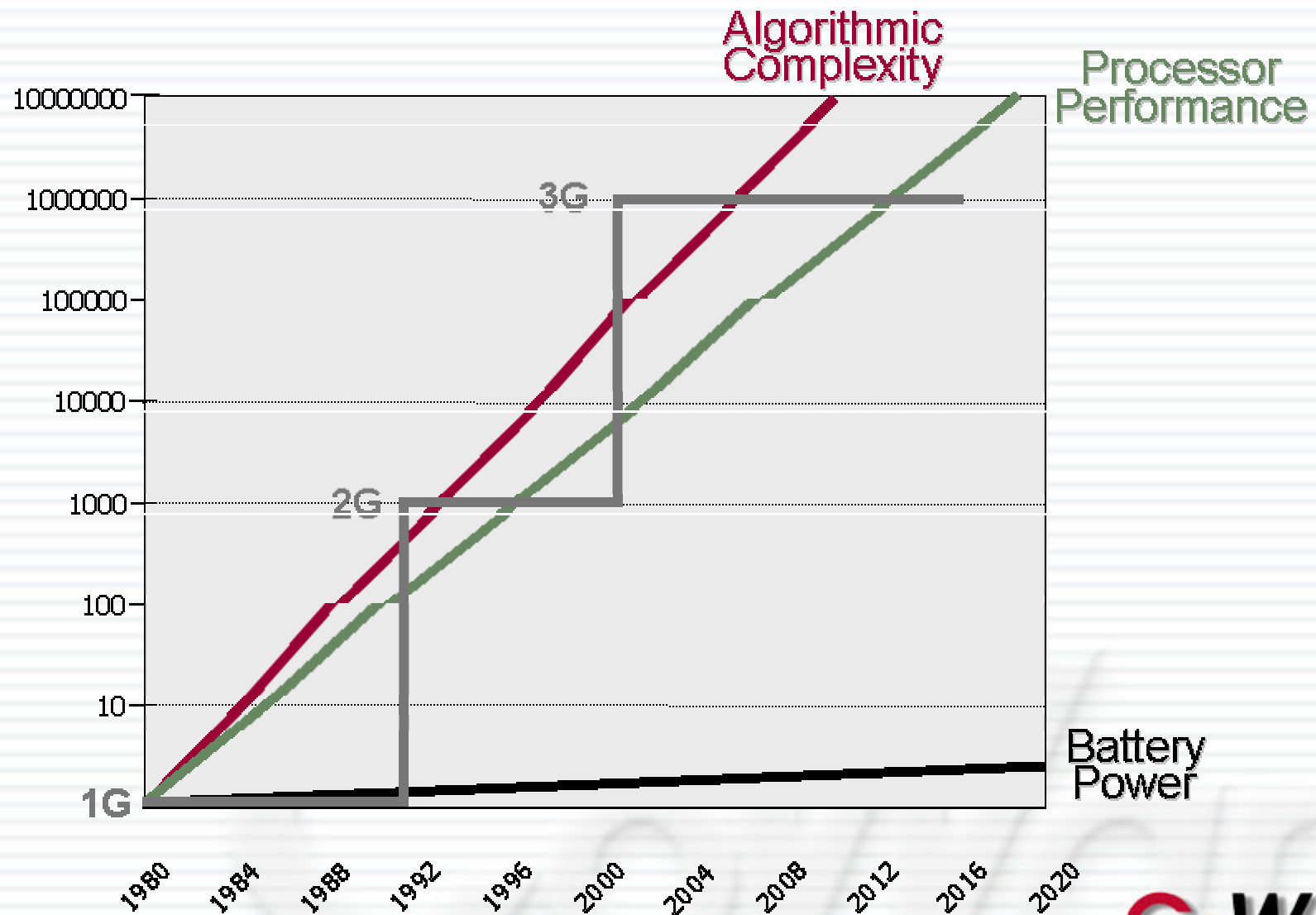
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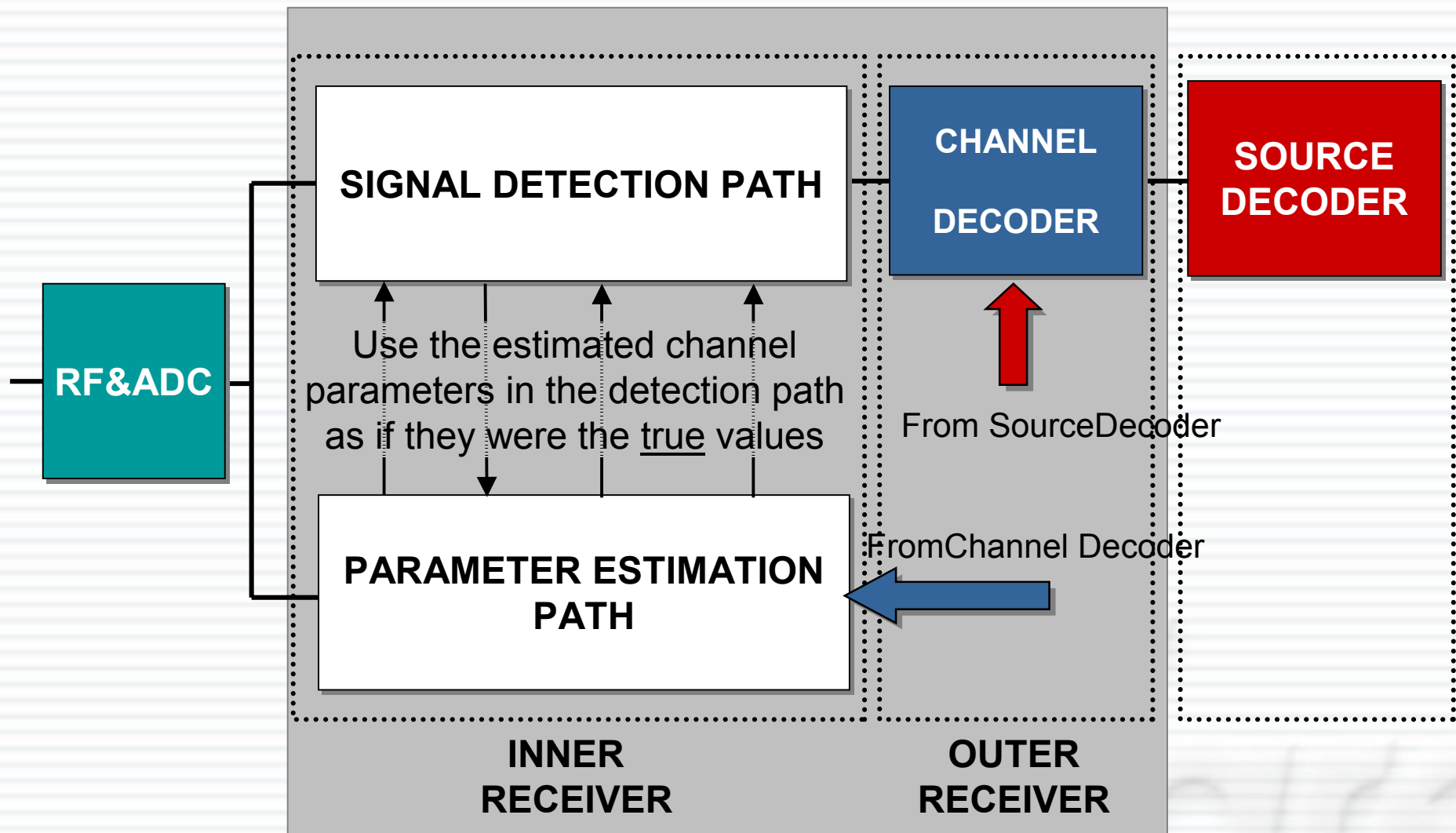
# Future Wireless Communication Systems

- Will be **adaptive, multifunctional** and **software definable** to optimally use the available bandwidth
- They will make use of **advanced signal processing** to achieve this goal..
  - Advanced compression algorithms for voice and video signals
  - Sophisticated algorithms for power control, channel estimation, interference cancellation, synchronization, decoding etc
  - Multiple antenna (MIMO)
  - Complex protocol to manage traffic in networks
  - User-friendly graphical man-machine interfaces
  - Voice recognition
- And process these algorithms on **heterogeneous configurable** computing engines

# The Algorithmic Driving Force



# Canonical Receiver Model



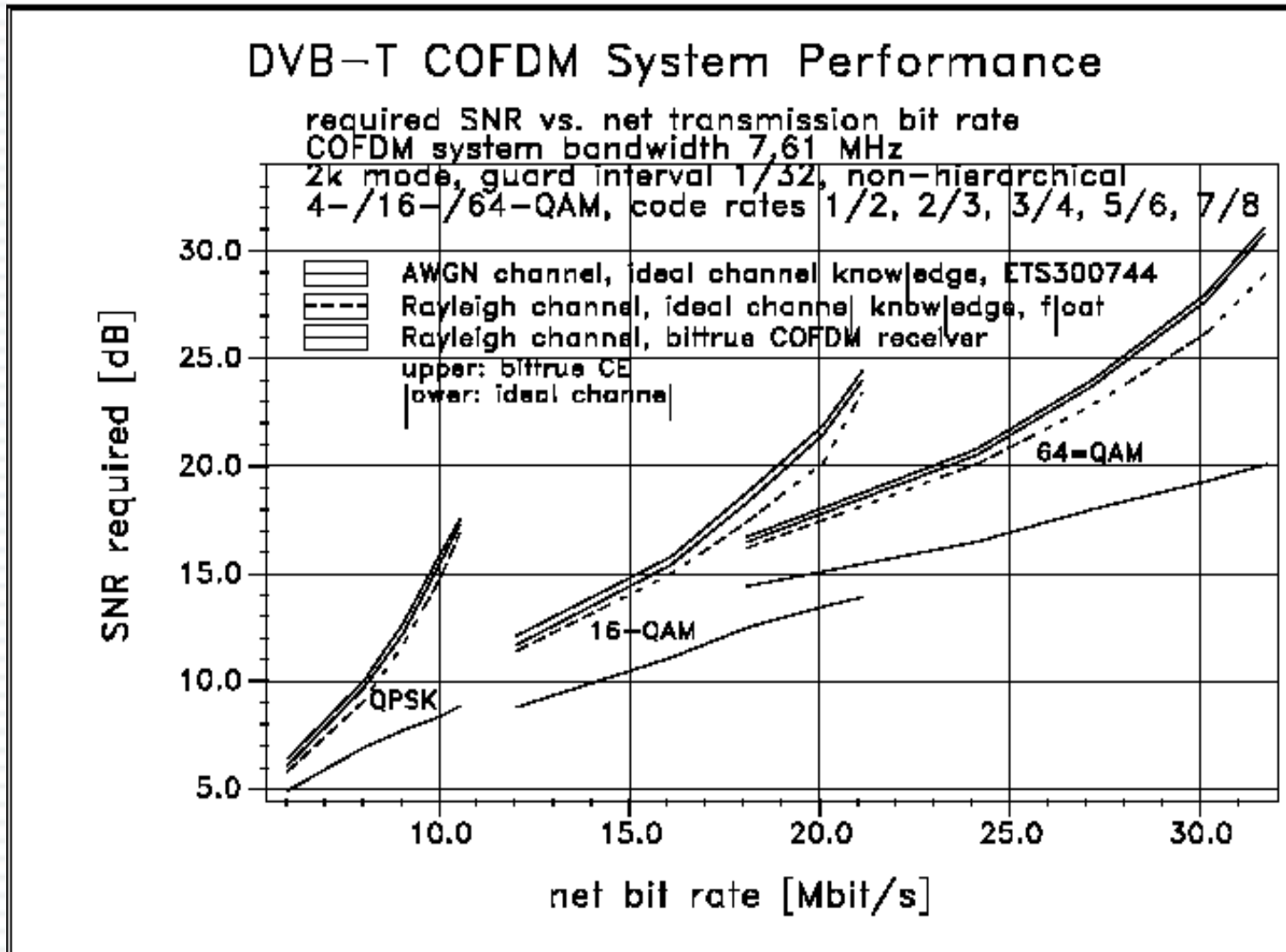
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# UWB - OFDM Allows...

- Application to frequency selective fading channels—it makes the channel look flat
- Highly-efficient digital implementation
- Adaptivity via modulation and coding
- Extension to MIMO

# Performance of DVB-T



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# Design Space: Architecture and Algorithm

## Inner Receiver

BOTH algorithm and architecture space exploration

***The algorithms of the inner receiver are never specified by the standard***

## Outer Receiver

ONLY architecture space exploration

***The decoder is exactly specified in the standard***

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# Multi-level SoC Design

- **System Application Design**
  - Algorithm design
  - C to C translation (S/W “washing machine”)
- **Multiprocessor SoC Platform Design**
  - Specification, assembly and reconfiguration of existing IP and interconnect structure
  - No IP blocks are designed
- **High-level IP Block Design**
  - ASIP design
  - Interconnect design with trend towards Network-on-Chip design
  - H/W IP (e.g. decoder)
- **Semiconductor Technology & Basic IP**
  - Standard cells, I/O, memories and basic technology processes

Source: P.Paulin, DAC 2003

# Multi-level SoC Design

- **System Application Design**

- Algorithm design
- C to C translation (S/W "Virtual Machine")

- **Multiprocessor SoC**

- Specification, synthesis, and verification of existing IP and interconnect
- No IP blocks

- **High-level IP**

- ASIP design
- Interconnect and on-chip design
- H/W IP (e.g. CoWare)

- **Semiconductor Technology**

- Standard cells, I/O, memories and basic technology processes

SPW

ConvergenSC

LISATek