CoWare Customer Success

Infineon Technologies Slashes Design Customization Time By 50% Using CoWare Processor Designer Automated Embedded Processor Design Environment

Customer Profile

Infineon Technologies' Advanced Systems and Circuits (ASC) Group develops algorithms for signal and protocol processing systems. The ASC Group designs application-specific processors, low power memory architectures and embedded field programmable devices to implement these algorithms. The ASC Group deploys approximately two-thirds of its effort in project-specific development for Infineon's product groups, while the remainder is engaged upon advanced technology research and development. The ASC Group thus stands at the nexus of state-of-the-art product design and technology development.

Business Challenge

The business challenge was to significantly increase design productivity to the level necessary to develop application-specific instruction set processors (ASIP) with their associated software development tools within tight time to market deadlines. Meeting this design productivity challenge is critical to the exploitation of the burgeoning market for such devices – both custom and standard parts.

Design Objectives

The design objectives were to develop a high-productivity ASIP design methodology and to use it to customize an existing Application-Specific Multi-Rate DSP (ASMD) processor. The target application was a continuously variable-slope delta (CVSD) codec function, to be integrated into Infineon's Bluetooth platform.

Results

Using CoWare Processor Designer automated embedded processor design environment, the ASC team shipped the ASMD/CVSD netlist in two months – a 50% reduction over the estimated time using the established design methodology.

CoWare Processor Designer deliverables comprised the ASMD architecture modified to comprehend the requisite new functionality, the new instruction set simulator (ISS), the new software development tools and the new hardware description, all generated automatically by Processor Designer from a single "golden" processor model.

> "We have adopted the Processor Designer-enabled ASIP approach as a standard methodology because it reduces design time tremendously, and offers improved reusability, efficient verification techniques and a streamlined design methodology."
>
> – Steffen Buch
> Director, Advanced Systems and Circuits Group
> Infineon Technologies

Moreover, Infineon had commenced the project with two parallel design flows – Processor Designer and a traditional VHDL-driven RTL design methodology – but then switched to the Processor Designer flow as it rapidly proved its efficacy.

Design Approach

A previous CVSD design had been developed as dedicated non-programmable hardware, using a VHDL design flow. Redesign of this circuit to meet a significantly enhanced specification would have entailed tedious and time-consuming manual RTL modification, and may have threatened Infineon's time to market objectives. Infineon concluded that modification of its existing programmable ASMD core would require less time.

The existing ASMD core utilizes a shift-and-add architecture to realize various digital signal processing functions, such as filtering and Cordic. Its architecture allows customization via the modification of a VHDL package. Infineon estimated that the time required to modify this package for the CVSD application would have been four months. The team embarked upon this approach, but also used the project as an opportunity to evaluate CoWare Processor Designer.

CoWare Processor Designer delivers significant processor design productivity increases by simplifying design space exploration to determine the optimum architecture, and by automating the design of hardware, ISS and software development tools. In this project,

however, Processor Designer was evaluated on its ability to speed the modification of an existing processor design, using a "new design" methodology.

Design Scope

An Infineon designer undertook a two-day LISA 2.0 language training and studied Processor Designer sample processors for a week. Real facility with the language was attained "on the job".

Within four weeks of project start, Infineon had developed the first LISA 2.0 architecture model of the ASMD and automatically generated the ISS and software tools. Infineon then profiled the architecture with software to analyze and evaluate its performance. The analysis results enabled the team to refine the architecture, generating new ISS and tools at each refinement, and then generate the hardware description in SystemC-RTL language. See Figure 1.

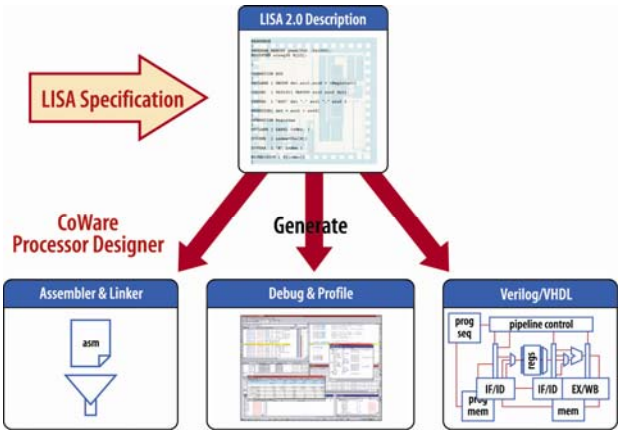

Figure 1: ASIP Design Methodology

Design space exploration with Processor Designer enabled the team to identify a significant performance improvement: the addition of a datapath and an instruction would enable the ASMD to execute CVSD step size control in 1 clock cycle – down from an estimated 17 clock cycles using the original architecture and instruction set. The architectural design was iterated, the RTL hardware description generated, the gate level netlist synthesized and verified, and the new software development tools generated – in *one day*.

By making all design iterations in the architectural model from which the ISS and RTL models are automatically generated, the methodology eliminates the errors often introduced by the manual, independent creation of individual models. However, the models must still be tested for compliance to specification. Consequently, Infineon verified and co-verified the LISA 2.0 model of the ASMD and the automatically-generated SystemC and RTL models in a system-level verification environment. Then, implementation-level compliance was tested with an extensive functional vector suite. See Figure 2.

In addition to traditional simulation techniques, Infineon utilized Processor Designer's ultra-fast Just-in-Time Cache Compiled (JIT-CC™) simulation. This enabled the team to execute multiple iterations and undertake extensive regression tests that may have been impractical using traditional simulation techniques alone.

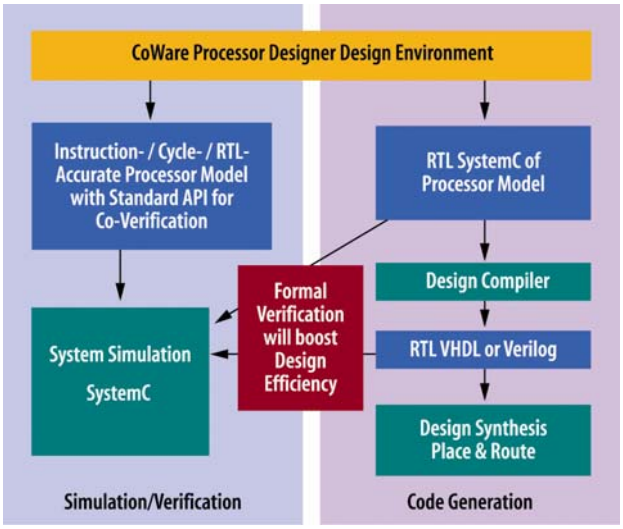

Figure 2: ASIP Verification Methodology

Infineon's Future Requirements

Infineon identified two significant improvement requirements. The first requirement – the automatic generation of a synthesizable RTL hardware description in Verilog or VHDL – is met by the latest release of CoWare Processor Designer. The second requirement – the elimination of model compliance simulation – may be met by emerging formal verification methods.

Conclusion

Using CoWare Processor Designer, Infineon slashed 50% from ASMD customization and software development tool generation time. Processor Designer also satisfied the detailed attributes of Infineon's methodology specification, such as applications profiling, short processor design iteration loops, one source for hardware and software views, a consistent verification environment, design reuse support and hardware implementation guidelines.

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