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An IP-based SoC Design Kit for Rapid Time-to-Market

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Abstract :

SuperH Inc., develops and licenses 32 and 64-bit CPU cores for use in System-on-Chip (SoC) devices. SuperH has developed an innovative set of tools to reduce the 'time to market' for licensees developing SuperH based SoC devices. A description of the SoC Evaluation and Design Kit (SEDK) is provided describing its main capabilities. These include providing (i) an early software development capability, (ii) "turnkey" integration capabilities of CPU core and interconnect components, and (iii) a rapid hardware prototyping capability based on FPGAs for realizing the users own IP.

An IP-based SoC Design Kit for Rapid Time-to-Market

i) Introduction: This paper presents the SoC Evaluation and Design Kit (SEDK) provided by SuperH. Further, the paper focuses on the leading edge front-end design capabilities of the SEDK.

SuperH is a world leader, with a proven track record in the design [1,2] and implementation [3,4] of high performance RISC processors.

The primary role of the SEDK is to provide SuperH customers with a modeling and hardware capability for evaluating and designing with the SuperH family of RISC cores and support peripherals for inclusion in their SoC products. Further, the kit allows the evaluation and design to be performed within short timescales.

The crucial role of achieving rapid time-to-market for company survival and commercial success has been well documented [5]. This paper focuses on the advanced design capabilities of the SEDK for achieving this goal. These features include:

- Providing the software team with the capability of developing code early in the design process. This avoids the software bottleneck problem (which in turn increases development time) of waiting until hardware is available before starting software development.
- Providing a "turnkey" process for the integration of the core, support peripherals and

interconnect of the customers design. This allows the customer to focus on their area of expertise in developing their IP. Hence a saving of effort and cost is achieved at reduced development timescales.

- Providing prototyping capability based on hardware. This is achieved with little effort and minimum timescales by realizing the core and its support peripherals on a SuperH evaluation chip and the User IP and its associated interconnect on FPGAs. This ensures User IP corrections can be rapidly evaluated.

The remainder of this paper is organized as follows: Section *ii* describes the primary design flow of the SEDK. Sections *iii to v* proceed presenting the three individual design packages included in the SEDK. Further, these Sections highlight their contribution to reducing development timescales. Conclusions of the work are described in Section *vi*.

ii) SEDK Primary Design Flow: The design (flow) process of refining a specification through simulation towards a HDL representation is now well established. This has been achieved through commercial [6] and open standard [7] EDA initiatives coupled with application by semiconductor manufacturers [8].

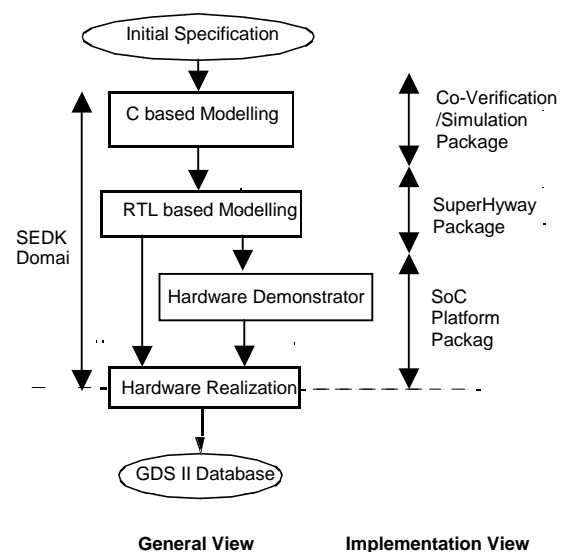


Fig. 1: SEDK Primary Design Flow

The SEDK maintains this methodology of lowering abstraction through its primary design flow. This is represented in Fig. 1.

The primary design flow is based on a generic or General View of refinement from Initial Specification to C-based Modeling to RTL-based Modeling and on to Hardware Demonstration and/or Realization. It is envisaged that this view will be stable over time.

The Implementation View indicates how the general view will be realized. This realization will evolve to react to developments at SuperH, contributions from EDA vendors and (most importantly) customer requirements. Currently the Implementation View is achieved using three individual design packages: Co-verification/Simulation Package, SuperHyway Package and the SoC Platform Package. These are described in the following Sections with reference to their capability to reduce development timescales.

iii) Co-verification/simulation Package: This package is concerned with C and RTL based modeling of the initial specification. The aim of the package is to refine the abstraction level of the model. This is represented in Fig. 2.

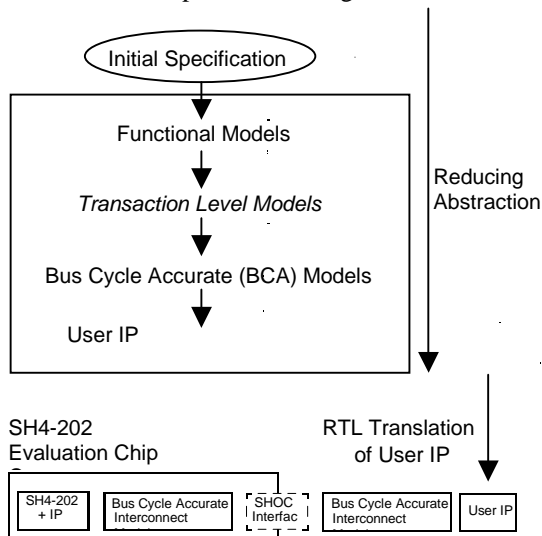


Fig. 2: Co-verification/simulation Package

The Functional Models are written in C/C++ and are coupled together using a functional router and interconnect. These allow rapid investigations with high simulation speeds. Currently, these investigations are carried out in the SystemC environment [9]. However, for some architectural investigations higher fidelity simulations are required. These are obtained by replacing the functional router and interconnect with a Bus Cycle Accurate (BCA) implementation. The SEDK currently uses the CoWare based SuperHyway [10] Toolkit initially developed by STMicroelectronics for the BCA interconnect. Further, the CoWare

design flow provides methodologies and tools for refining the User IP from C based models to RTL (Verilog/VHDL). The SuperHyway Off-Chip (SHOC) interface exists on the SH4-202 evaluation chip to allow access to the SuperHyway bus on the FPGA.

The SEDK will also implement Transaction Level Modeling (TLM) currently being promoted as a useful compromise between functional and BCA modeling [11].

The core model (assumed to be the SH4-202 in the context of this paper) is modeled as a cycle approximate model. Compilers for the SuperH cores are based on the freeware GNU tools, gcc/g++. Further, the GNU tool gdb is employed as the basis for the debugger interface.

One of the major benefits of the Co-verification/simulation package is that **software development can start early** in the project. This reduces the bottleneck problem of waiting until hardware is available. In addition, these modeling and development processes allow important system level design issues to be addressed. These include:

- Hardware/software partitioning,
- Software optimization, and
- Hardware realization.

Further, initial validation of the design can begin. Precise details of trade-off investigations and initial validation are outside the scope of this paper. When the system design has reached stability in simulation the process of hardware realization can proceed.

iv) SuperHyway Package: The SuperHyway is a flexible, high-performance on-chip interconnect with direct support for advanced IP cores. The SuperHyway protocol is based on packet routing technology and is often likened to a silicon network rather than a simple bus. SuperHyway implementations can vary in topology, width, frequency, arbitration policy etc. A consequence of this is that SuperHyways can be highly optimized for a particular SoC's area, floorplan, performance constraints. The SuperHyway package gives an extremely simple way of specifying SuperHyways and a powerful tool which will automatically generate synthesizable RTL from this. In addition the package contains a functional verification tool which is able to validate the routing, arbitration and performance characteristics of the design.

The SuperHyway package gives the user of two tools with which they can specify and generate the interconnect. The first is based on employing a GUI to assist in the process. This method uses the Core Tools family (CoreDeveloper, CoreBuilder and CoreConsultant) from Synopsys to generate, synthesize and validate the interconnect design. This package follows its own design flow documented in [12]. The use of these tools

provides **turnkey processing of SuperHyway interconnects** through use of friendly GUIs and automation of tasks (such as connectivity) previously carried-out by hand.

The tool is based on using RTL templates and scripts to generate, synthesize and validate the interconnect.

Validation is based on generating transaction sequences communicated between initiators and targets within the interconnect design and assessing protocol compliance. The capability to generate random, deterministic and combination sequences is provided. Further, the user may perform directed testing that aids focusing on a particular part of the design. Among other tools the SEDK contains a virtual component specified in SPECMAN from verisity. This also allows verification coverage statistics to be retrieved relatively easily.

The output of the SuperHyway Package is a fully validated interconnect associated with the User IP. This is implemented in RTL and can be employed in a HDL simulator (for example, NCSIM by Cadence). A simple application of the SuperHyway Package design is represented in Fig. 3:

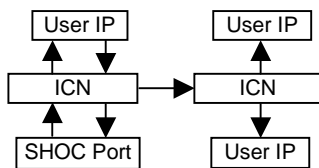


Fig. 3: Application of the SuperHyway Package Interconnect Design

Here the arrows indicate the initiator target connectivity to User IP and interconnect nodes (ICN).

Example

The outputs of the Co-simulation/verification Package and SuperHyway Package can be linked for more precise validation tests. This is represented in Fig. 4 for the case of a design based on the SH4-202 evaluation chip.

Here the major components of the SH4-202 Evaluation chip are highlighted. These include the memory modules: external memory interface (EMI), and flash EMI (FEMI), the core support peripherals (CSP): clock/power mode generator (CPG), timer module (TMU), real-time clock (RTC), interrupt controller (INTC), and the serial communications interface with FIFO (SCIF). A second set of peripherals, the external peripherals bridge (ePBR) is included to provide additional services for the User IP as required. The design is now ready to be realized in hardware.

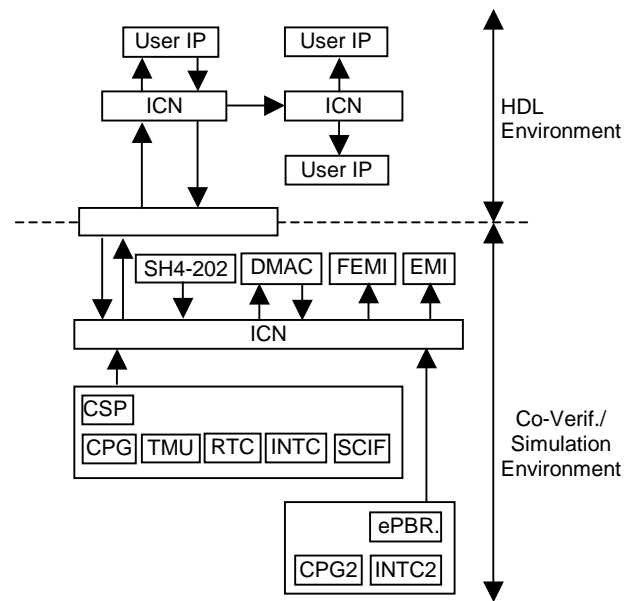


Fig. 4: Co-verification/Simulation – SuperHyway Packages

v) SoC Platform Package:

The SEDK includes a SOC design platform which has 3 primary uses:

- A platform for software development
- An application demonstrator platform
- An SoC prototyping platform

The structure of the platform is modular which allows very powerful systems to be developed but also permits very low cost access for users with more limited aims.

The major components of the package consist of an SH4-202 evaluation chip coupled to a FPGA via a SHOC interconnect. In addition, all tools required to realize the design in hardware are provided. Further, the use of the Co-verification/simulation and SuperHyway Packages can be directly applied to the SoC Platform Package. Therefore, a direct mapping onto the hardware exists. This is shown in Fig. 5.

This provides a **hardware prototyping capability** that is implemented with little effort in short timescales. Further, corrections or modifications to the User IP or associated interconnect can be carried out quickly on the FPGA.

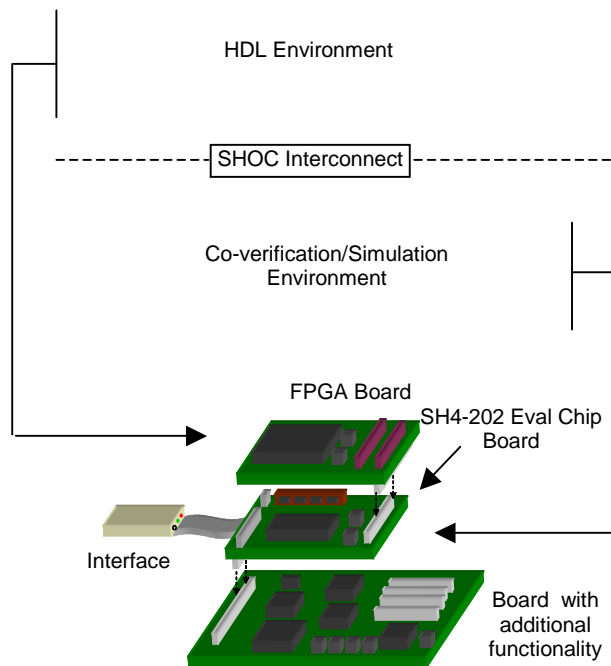


Fig. 5: Hardware Mapping

vi) Conclusion: This short paper has provided an overview of the SoC Evaluation and Design Kit (SEDK) produced by SuperH Inc. The primary role of the kit is to provide SuperH customers with a modeling and hardware capability for evaluating and designing with the SuperH family of RISC cores and support peripherals for inclusion in their SoC products. In addition, this role is to be achieved in short timescales ensuring the customer can achieve rapid time-to-market.

Three main capabilities that contribute to reducing development timescales have been presented:

- Early software design capability is provided through modeling in the Co-verification/simulation Package. This allows code development to begin with the functional model. The software can then be refined through various stages of development through to prototyping. This avoids the software bottleneck problem of waiting to start code development until hardware is available.
- Turnkey integration capabilities are provided for core, its support peripherals, and the interconnect. The SEDK design flow and SuperHyway Package ensure this capability. The SuperHyway Package deals with the interconnect associated with the User IP. The design flow ensures that the core, its support peripherals and associated interconnect are mapped on to the evaluation chip. This allows the customer to focus on their area of expertise, i.e. the User IP while reducing the effort and time associated with other integration issues.

- Hardware prototyping capabilities that require little effort and minimum timescales are provided. These are provided by the SEDK design flow and the SoC Platform Package. The design flow ensures that the User IP and its associated interconnect are mapped on to the SoC Platform Package FPGAs while the core, its support peripherals and associated interconnect is mapped on to the evaluation chip. In addition, this ensures that re-designs can be carried-out in short timescales.

Our future work will focus on evolving the SEDK in response to developments by SuperH, EDA vendors, hardware suppliers, and most importantly customer requirements.

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References:

- [1] A. Hasegawa, M. Debbage, A. Sturges *et al*, "SH-5: The 64-bit SuperH Architecture", IEEE Micro, July/August 2000.
- [2] R. Curnow, M. Hill and A. Jones, "An Embedded Processor Architecture with Extensive Support for SoC Debug", IP Based SoC Design'2002, Paper Id 53, October 2002.
- [3] <http://www.superh.com>, "SuperH Inc Homepage".
- [4] http://www.hitachisemiconductor.com/sic/jsp/japan/eng/products/mpumcu/32bit/superh/sh7751_e.html, "SuperH Family – Processor Type".
- [5] J. Borel, "Design Automation in MEDEA: Present and Future", IEEE Micro, Sept-Oct 1999.
- [6] CoWare Inc., "CoWare N2C Methodology Manual", Version 3.1, July 2001.
- [7] <http://www.systemc.org>, "SystemC Version 2.0 User's Guide", 2002.
- [8] B. Clement *et al*, "Fast Prototyping: a system design flow applied to a complex SoC multiprocessor design", DAC 99, New Orleans, July 1999.
- [9] <http://www.systemc.org>, "SystemC Homepage"
- [10] A. Jones and J. Carey, "SuperHyway provides SoC backbone", <http://www.eetimes.com/story/OEG20001023S0063>
- [11] A. Clouard, "Experiences and Challenges of TLM in SystemC v2.0", <http://www.systemc.org>.
- [12] P. Butta *et al*, "Leveraging Soft IP in an Enhanced Integration Flow", SNUG Europe, 2002.