

The LISATek™ Solution

Automated Embedded Processor Design and Software Development Tool Generation

LISATek is an automated embedded processor design and optimization environment that slashes months from processor hardware design time and engineer-years from the creation of processor-specific software development tools. LISATek's high degree of automation enables even those design teams with no processor development expertise to create advanced processors. Moreover, it generates software development tools for processors that have not been designed using LISATek's automated hardware design capability.

LISATek dramatically accelerates the design of both custom and standard processors, including the application-specific instruction set processors (ASIPs) that are increasingly essential to convergent system-on-chip (SoC) functionality. LISATek is used to develop any of a wide range of processor architectures, including DSP, RISC, SIMD, VLIW and superscalar.

LISATek's generated software development environment enables the commencement of application software development prior to silicon availability, thus eradicating a common bottleneck in embedded system development.

The key to LISATek's automation is its Language for Instruction Set Architectures, LISA 2.0. LISA 2.0 enables the creation of a

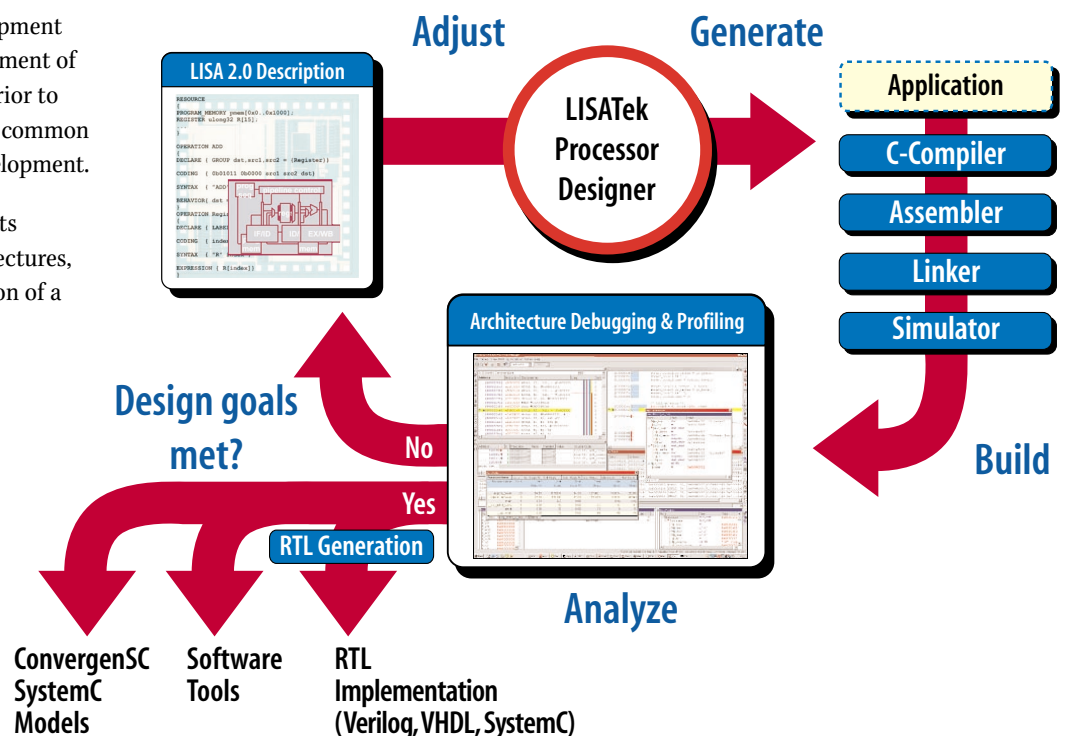
single "golden" processor model as the source for the automatic generation of the instruction set simulator (ISS), the complete suite of software development tools, and synthesizable RTL code. The development tools, together with the extensive profiling capabilities of the software simulator and debugger, enable rapid exploration of the processor architecture instruction set to determine the optimal architecture for the target application domain. LISATek enables the designer to optimize instruction set design, processor micro-architecture and memory systems, including caches.

LISATek's use of a single processor model source ensures the compatibility of the ISS, software tools and RTL implementation, eliminating the verification and debug effort necessitated by multiple independently created models with different levels of abstraction.

H I G H L I G H T S

- Integrated design environment for unified processor design and software development tool generation – with no processor design expertise required
- Slashes processor hardware design time by months
- Eliminates engineer-years from software tool generation effort—even for processors not designed with LISATek
- Ensures compatibility of ISS, software tools and RTL implementation
- Software development environment enables application software development prior to silicon availability

Operating at a high level of abstraction, LISATek not only eliminates the time and cost inherent in HDL-based processor design and manual tool development, but also enables processor design by non-experts.



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Key Features

- Single, cohesive environment for the modeling, exploration and design of the processor architecture.
- Automatic generation of fast and accurate ISS, both instruction- and cycle-accurate.
- Simulator performance improved by up to 60% and memory usage reduced by up to 50% over previous releases.
- Extensive profiling capabilities for the ISS, micro-architecture and memory enable optimization for speed, area and power consumption.
- Automatic generation of synthesizable RTL
 - Control and datapath
 - VHDL and Verilog
 - Compatible with established synthesis tools and flows
 - Single data source ensures consistency of RTL with ISS, while co-validation verifies conformance of RTL behavior with ISS behavior
- Automatic software development tool generation
 - Optimizing C-Compiler
 - Standard library support (libc)
 - Symbolic debug data
 - Comprehensive automated code optimization
 - Compiler validation suite
 - Binary code generation tools comprising rich macro-assembler, dis-assembler, linker and archiver
 - Integrated profiling enables software optimization with the target architecture, comprehending memory and micro-architecture.
 - Instruction Set Simulation
 - Ultra-fast, Just-in-Time Cache Compiled (JIT-CC™) simulation (patent pending)
 - Processor Support Package (PSP) generation for SystemC-based system-level design environments such as CoWare ConvergenSC and the Open SystemC Initiative (OSCI) Reference Simulator
- Instruction and data trace generation
- Enables easy integration with other third-party debuggers
- Comprehensive debug options
 - Graphical debugger enables symbolic debug of C/C++ application software with the target architecture and micro-architecture, with extensive profiling capabilities that support optimization of software and hardware
 - Multi-core debugger enables software debug with multiple cores in a system verification environment such as CoWare's ConvergenSC and the OSCI Reference Simulator, or in an HDL/C co-simulation tool, such as Mentor's Seamless
 - Interactive source level debug of the LISA 2.0 processor description
- LISATek embedded software development environment
 - Enables the commencement of application software development prior to the availability of silicon, and the very fast execution and validation of large amounts of application code
 - Deploys LISATek's optimizing C-compiler, binary code generation tools, a very high speed ISS, and an integrated debug environment
 - ISS is an order of magnitude faster than comparable simulators, as measured on a 2.5GHz Athlon PC
 - 5 to 30 MIPS for instruction-accurate models
 - 0.5 to 5 MIPS for cycle-accurate models
- Supported Platforms
 - Solaris 8, Solaris 9
 - Red Hat 8.0
 - Red Hat Enterprise Linux 3
 - Windows XP Professional* (*C-Compiler generation not available for Windows)

Major Benefits

- Enables design teams—even non-experts—to rapidly develop flexible and re-usable embedded processors, including those essential to convergent SoC functionality, through:
 - Rapid architecture design with LISA 2.0 by any designer conversant with C/C++
 - Automatic generation of models and software development tools
 - Easy instruction set profiling and optimization to meet or beat performance objectives
 - Automatic generation of synthesizable RTL for both control and datapath hardware, with robust links to established RTL simulation and synthesis tools
 - A unified, automated methodology that ensures consistency of hardware and software implementations with the high level design models
- Enables embedded software application development and debug with greatly reduced time to market through:
 - Early commencement of software development before silicon availability
 - Reduced software application design and development time
 - Fast and accurate instruction set simulator



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