

CoWare® SPW Library for Xilinx LTE IP

Improving Wireless Design Productivity for LTE Basestation Design

SPW Wireless Reference Libraries

SPW Wireless Reference Libraries provide an unmatched increase in productivity for wireless physical layer system design. They can be used by network operators for investigation of system performance both for scenarios specified in the standard as well as in corner cases relevant to optimize network performance and cost. For basestation and handset modem design teams, the SPW library not only provides a reference model for validation of their specifications, but the provided source code also provides very valuable insight into the standards definition, which may otherwise require months of perusing the pertinent documents. Also the source code can be used as a starting point for today's mostly processor based implementation of wireless systems.

The reference models provide ideal receivers (with perfect knowledge of the channel) and non-ideal receivers (which must estimate the channel characteristics). The ideal receiver provides the maximum achievable performance for comparison against real and non-ideal receiver implementations.

Wireless Reference Libraries are organized into specific regression test benches which mirror the tests being specified in the standards reference documents. The user can immediately run these regressions and easily modify system parameters of interest in order to study performance impact. By replacing or modifying blocks or subsystems the user can quickly adapt the reference to the specific implementation for the end product. The ability of SPW to start as many regression simulations as possible, limited only by the server infrastructure at hand, provides wireless designers using the Reference Libraries with unmatched exploration opportunities,

hence improving product performance with the time-to-market window.

The Wireless Reference Libraries can be used for block level verification of hardware and software components. HDL Cosimulation as well as target code simulation either on the host or using an Instruction Set Simulator (ISS) for the target processor enables the use of the library as a verification environment.

The Wireless Reference Libraries are developed by a team of wireless system designers that collectively have 50+ years of wireless design expertise. They are validated against available references from the standard test equipment as well as with lead customers.

SPW Library for Xilinx LTE IP

Xilinx provides IP components that allow basestation manufacturers to reduce implementation time for LTE systems implemented on Xilinx programmable devices. The implementation of these IP components is optimized for device performance such as power consumption and resource utilization.

Xilinx also provides bit-accurate C reference models that can be used for IP optimization and system verification by users integrating the Xilinx LTE IP models within their design. Using the prepackaged models from the SPW Library for Xilinx LTE IP library allows for easy integration into the CoWare LTE Reference Library, which is sold as a separate option. This allows the user to evaluate the system throughput using the Xilinx IP in conjunction with their own LTE IP and algorithms. Furthermore, since the Xilinx IP models are bit-accurate, they can also be part of a verification testbench for the entire system as well being exported to become part of a Virtual Platform for software verification.

Turbo Decoder

For complete details, see the [Xilinx data sheet](#).

The Xilinx 3GPP LTE Turbo Decoder is an optimized core designed to fulfill the requirements described in the 3GPP LTE specification TS 36.212. The core has several parameters which may be optimized to fulfill conflicting performance, power and resource requirements.

Key Xilinx IP Features

- Fully compliant to the 3GPP LTE specifications TS 36.212
- Throughput greater than 200 Mbps using 8 decoders
- Intelligent scheduler allocates tasks across available decoder units to optimize throughput and latency

Model Parameters

- Number of parallel decoding units: 1, 2, 4, or 8
- Decoding algorithms: MAX (Max Log-Map), MAX scale (Max Log-Map with external scaling) or MAX* (Log-Map)
- I/O integer bit width: 4 or 5 (fractional bit width fixed at 3 bits)
- Number of iterations: 1–15

MIMO Decoder

For complete details, see the [Xilinx data sheet](#).

The Xilinx 3GPP LTE MIMO Decoder is an optimized core designed to perform Multiple Input Multiple Output decoding using the Minimum Mean Square Estimation (MMSE) algorithm.

Key Xilinx IP Features

- Fully compliant to the 3GPP LTE specifications TS 36.211 v8.5
- MMSE based algorithm
- Support for MU-MIMO and SU-MIMO with 2 transmit antennas
- Support for up to 20MHz FDD and TDD systems

Model Parameters

- Number of transmit antennas: 1 or 2
- Number of receive antennas: 1, 2 or 4

Please ask your CoWare representative for the current roadmap of additional models

Customer Focus

CoWare provides a complete range of training, support, design methodology consulting, and integration services. Technical support requests are handled directly by experienced design engineers who are fully familiar with the application of CoWare tools and methodologies to real-world designs. Training courses are available at CoWare offices or at the customer site and can be tailored to meet the specific needs of the design team.

Sales Offices

CoWare has sales offices in the U.S., Europe, Asia Pacific and Japan. For a complete listing with contact information visit www.coware.com. For technical or sales information call 1-888-CoWare8 or email info@coware.com.



CoWare, Inc.

Corporate Headquarters

1731 Technology Drive, Suite 200
San Jose, CA 95110

Main: 408-392-8500

Fax: 408-392-8601

www.CoWare.com