

CoWare® Processor Designer

Programmable Accelerators for Platform-Driven ESL Design

CoWare® Processor Designer is an automated, application-specific embedded processor design and optimization environment that slashes months from processor hardware design time and engineer-month from the creation of application processor-specific software development tools. Processor Designer's high degree of automation enables design teams to focus on architecture exploration and application-specific processor development, rather than on consistency checking and verification of individual tools.

Processor Designer dramatically accelerates the design of both custom processors and programmable accelerators, including the application-specific instruction set processors (ASIPs) that are increasingly essential to convergent system-on-chip (SoC) functionality. Processor Designer is used to develop a wide range of processor architectures, including architectures with DSP-specific and RISC-specific features as well as SIMD and VLIW architectures.

Processor Designer's generated software development environment enables the commencement of application software development prior to silicon availability, thus eradicating a common bottleneck in embedded system development.

The key to Processor Designer's automation is its Language for Instruction Set Architectures, LISA 2.0. In contrast to SystemC, which has been developed for efficient specification of systems, LISA 2.0 is a processor description language that incorporates all necessary processor-specific components such as register files, pipelines, pins, memory and caches,

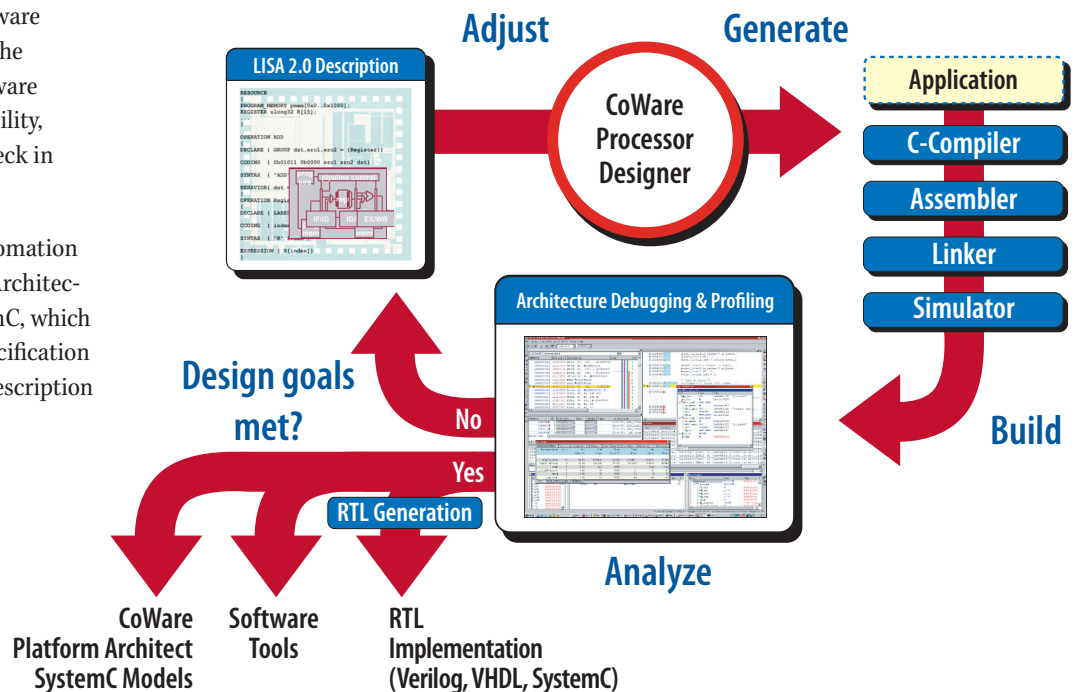
and instructions. It enables the efficient creation of a single "golden" processor specification as the source for the automatic generation of the instruction set simulator (ISS) and the complete suite of software development tools, like Assembler, Linker, Archiver and C-Compiler, and synthesizable RTL code. The development tools, together with the extensive profiling capabilities of the debugger, enable rapid analysis and exploration of the application-specific processor's instruction set architecture to determine the optimal instruction set for the target application domain. Processor Designer enables the designer to optimize instruction set design, processor micro-architecture and memory sub-systems, including caches.

Processor Designer's use of a single high-level processor specification ensures the consistency of the ISS, software development tools and RTL implementation, eliminating the verification and debug effort necessitated by multiple, independently-created models.

H I G H L I G H T S

- Integrated design environment for unified application specific processor, programmable accelerator design and software development tool generation
- Slashes application specific processor and programmable accelerator hardware design time by months
- Eliminates months of engineer-effort for software tool development
- Ensures compatibility of instruction set simulator (ISS), software development tools and RTL implementation
- Software development environment enables application software development prior to silicon availability

Operating at a high level of abstraction, Processor Designer not only eliminates the time and cost inherent in HDL-based processor design and manual tool development, but also enables hardware and software designers to customize the instruction set to their needs.



Key Features

- Single, cohesive environment for the modeling, exploration and design of application specific processors and programmable accelerators.
- Automatic generation of high speed and accurate ISS, both instruction- and cycle-accurate.
- Extensive profiling capabilities for the ISS, micro-architecture and memory enable optimization for speed, area and power consumption.
- Automatic generation of synthesizable RTL
 - Control and datapath
 - VHDL and Verilog
 - Compatible with established synthesis tools and flows
 - Single data source ensures consistency of RTL with ISS, while co-validation verifies conformance of RTL behavior with ISS behavior
- Automatic software development tool generation
 - Optimizing C-Compiler
 - Standard library support (libc)
 - Symbolic debug data
 - inline assembly support
 - Comprehensive automated code optimization
 - Compiler validation suite
 - Binary code generation tools comprising rich macro-assembler, dis-assembler, linker and archiver
 - Integrated profiling enables software optimization with the target architecture, comprehending memory and micro-architecture.
- Instruction Set Simulation
 - Ultra-fast, Just-in-Time Cache Compiled (JIT-CC™) simulation (patent pending)
 - Processor Support Package (PSP) generation for SystemC-based system-level design environments
 - Instruction and data trace generation
 - Enables easy integration with other third-party debuggers
- Comprehensive debug options
 - Graphical debugger enables symbolic debug of C/C++ application software with the target architecture and micro-architecture, with extensive profiling capabilities that support optimization of software and hardware
 - Multi-core debugger enables software debug with multiple cores in a system verification environment such as CoWare Platform Architect and the OSCI Reference Simulator, or in an HDL/C co-simulation tool
 - Interactive source level debug of the LISA 2.0 processor description
- Processor Designer embedded software development environment
 - Enables the commencement of application software development prior to the availability of silicon, and the very fast execution and validation of large amounts of application code
 - Deploys Processor Designer's optimizing C-compiler, binary code generation tools, a very high speed ISS, and an integrated debug environment
- Supported Platforms
 - Solaris 8, Solaris 9
 - Red Hat 8.0
 - Red Hat Enterprise Linux 3
 - Windows XP Professional* (*C-Compiler generation not available for Windows)

Major Benefits

- Enables design teams to rapidly develop flexible and re-usable application specific embedded processors, including those essential to convergent SoC functionality, through:
 - Rapid architecture design with LISA 2.0 by designers conversant with C/C++
 - Automatic generation of simulator and software development tools
 - Easy instruction set profiling and optimization to meet or beat performance objectives
 - Automatic generation of synthesizable RTL for both control and datapath hardware, with robust links to established RTL simulation and synthesis tools
 - A unified, automated methodology that ensures consistency of hardware implementation, simulation model and software development tools implementations with the high level design specification
- Enables embedded software application development and debug with greatly-reduced time to market through:
 - Early commencement of software development before silicon availability
 - Reduced software application design and development time through higher visibility and comprehensive debugger
 - Fast and accurate instruction set simulator



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