

WCDMA Library

Accelerating Wireless Design Productivity For 3G Cellular System Design

Overview

Code-division multiple access, or CDMA, technology is the foundation for many modern wireless communications systems. To assist engineers designing Wideband CDMA (WCDMA) systems, CoWare has developed a WCDMA library for Signal Processing Designer. Use of SPD's WCDMA library can expedite your design of WCDMA systems by facilitating algorithmic exploration and shortening development and design verification times. It also can increase your chance of first-time design success. You can also combine WCDMA library models with other Signal Processing Designer models. For example, by combining WCDMA models with models from SPD's multimedia library, a designer can quickly build advanced 3G wireless system level designs which include multimedia (video) features.

History

The Signal Processing Designer team has been producing end-to-end physical layer baseband simulation models of third generation WCDMA standards since December 1997. This effort started with UMTS and ARIB WCDMA and was followed by 3GPP and 3GPP2 models. CoWare continues to track the evolving standards and uses information from the standards committees to build the system level models. The models, in turn, provide a framework and a testbench for users interested in hardware and/or software implementation of all or parts of a 3G design.

The WCDMA Library

The system level models provided by the WCDMA library include many baseband processing functions. The following lists several functions available in the library.

- Transmitter modeling functions including variable rate data generation, channel coding (both convolutional and turbo), rate matching single or multicarrier spreading, scrambling, and transmit filtering
- Channel/environment modeling functions including a Wideband Rayleigh fading channel model (up to six paths) with log-normal shadow fading and additive white Gaussian noise (AWGN)
- Receiver modeling functions including receiver filtering, rake receiver (up to six fingers), descrambling, despreading, de-rate-matching and channel decoding (both Viterbi for convolutional codes and Maximum A-Posteriori (MAP) for turbo codes)
- Performance analysis functions including bit error rate (BER) and frame error rate (FER) counting

The Signal Processing Designer environment allows users to replace parts of these system models with their own hardware or software implementations and then simulate their implementation in the context of the entire system. This provides a powerful environment to rapidly develop, debug, and validate an implementation.

The 3GPP models provide both ideal receivers (with perfect knowledge of the channel) and non-ideal receivers (which must estimate the channel characteristics). The ideal receiver gives a best case scenario for comparison against your real and non-ideal receiver design.

The WCDMA library covers the Frequency Division Duplex (FDD) of the 3GPP standard. CoWare's strategy is to rapidly update the libraries as the recommendations evolve and become standards. We are committed to the continued updating of these models until they reach their final maturity.

H I G H L I G H T S

- Supports the design of 3GPP Wideband CDMA (WCDMA) products
- Includes a rich set of libraries of fundamental CDMA functions such as sequence generation, spreading and despreading operations
- Provides several CDMA and WCDMA system test benches
- Includes fixed-point algorithmic design capture and datapath performance analysis
- Enables simulation of C, C++, and/or HDL blocks in a single simulation process
- Conforms to current standards for 3GPP WCDMA
- Accelerates complete design of a 3G wireless personal device when used with optional Signal Processing Designer libraries such as the WLAN library for IEEE802.11, and Bluetooth
- Compatible with the Signal Processing Designer Multimedia Library for the development of 3G systems that incorporate imaging/video subsystems such as a digital camera, video compression routines, and/or video display

WCDMA Verification Systems

The WCDMA library includes a number of system reference models. The testbench models can be used for algorithmic exploration of an end-to-end WCDMA system. These reference systems model all aspects of a CDMA system, including sequence generation, acquisition, tracking, channel estimation, and interference cancellation. Each modeled system is configurable, enabling users to make rapid modifications to support modeling their particular WCDMA system design decisions.

The 3GPP WCDMA reference systems included in the library are as follows:

Downlink Channel

This system models an end to end single code 3GPP downlink system with two transport channels in its standard configuration,

but is flexible enough to allow as many or as few transport channels as wanted. This reference system can be used to verify the DCH demodulation performance requirements in 3GPP TS 25.101 sections 8.2, 8.3, 8.4 and 8.5. The standard 12.2kbps, 64kbps, 144kbps and 384kbps measurement channels can easily be simulated by changing a single parameter. The receiver model is ideal. A similar system supporting Space Time Transmit Diversity is also available.

Transmitter Model Details

- Transport channel generation and coding
- Primary and secondary synchronization channels
- Common pilot channel
- Primary common control physical channel
- Page indication channel
- 16 channel orthogonal channel noise simulator
- Compressed mode with puncturing, spreading factor reduction, higher layer scheduling modes
- Both A and B compressed mode frame structures
- Fixed and flexible frame positions
- Transport format combination indicator coding
- Pilot symbol generation
- Turbo and convolutional coding
- CRC generation
- First and second interleaver
- Scrambling code generation
- OVFSF code generation

Channel Model Details

- Static, fading cases 1 through 6, moving and birth-death channel conditions

Receiver Model Details

- Ideal receiver model
- Compressed mode support
- First and second deinterleaver
- CRC checking
- Transport format combination indicator decoding
- Turbo code scaling

- Viterbi decoder
- Turbo decoder
- Rate de-matcher
- Block error rate and bit error rate measured

Downlink HSDPA

This model implements the High Speed Downlink Packet Access channel introduced in Release 5 of the 3GPP standard. It has QPSK and 16QAM modulation modes and can be used to verify the HS-DSCH Fixed Reference Channel performance requirements in 3GPP TS 25.101 section 9.2.1. Both the HS-DSCH and the HS-SCCH channels are implemented and the receiver uses information from the HS-SCCH to decode the data on the HS-DSCH. It models the HARQ protocol with ACK/NACK feedback and soft combining. Turbo coding (HS-DSCH) and convolutional coding (HS-SCCH) are fully supported.

Transmitter Model Details

- Transport block generation with support for up to 8 HARQ processes and changeable transmit pattern
- HS-DSCH bit scrambling
- Turbo coding with support for multiple code blocks (HS-DSCH)
- Convolutional coding (HS-SCCH)
- Rate matching (HS-DSCH and HS-SCCH)
- HS-DSCH interleaving and constellation rearrangement
- HS-SCCH frame generation
- HS-DSCH multi-code transmitter supporting both 16QAM and QPSK modulation

Channel Model Details

- Standard 3GPP model with PA3, PB3, VA30 and VA120 as preset propagation conditions

Receiver Model Details

- HS-SCCH ideal receiver
- HS-DSCH ideal multi-code receiver model supporting both 16QAM and QPSK modulation
- HS-DSCH deinterleaving and rate dematching
- HARQ soft combining
- Turbo (HS-DSCH) and Viterbi (HS-SCCH) decoding

- MACK/NACK generation
- HS-DSCH throughput measured

Downlink Practical Rake Receiver

The downlink Practical Rake receiver system is the same as the Downlink Channel reference system, with the exception of the Ideal Receiver which has been replaced by a Practical Receiver model. The Practical Receiver model has the following features:

- Pilot-based rake receiver integrated with full downlink system
- Four rake fingers modeled with support of up to six fingers
- Maximum ratio combining
- Channel delay tracking loop
- Coherent tracking using Common Pilot Channel (CPICH)
- Fully polymorphic for fixed-point exploration
- Fixed point RTL version available as well

Downlink Practical Rake Receiver— RTL Implementation

This is same as the above system except that the Practical Rake Receiver has been refined for Fixed-Point simulation and Hardware (RTL) generation. It is implemented using HDS, Advanced HDS and CDMA RTL library blocks. The RTL Implementation of Practical Rake Receiver design has the following features:

- Fixed-point refinement (bitwidths and modes) of the design
- Fixed-point simulation functionally matches the floating-point design
- Hardware refinement of the design by adding clocks, adjusting delays, removing multirate blocks and adding extra control circuitry
- Hardware generation from the design outputting synthesizable Verilog and VHDL which can map to both ASICs and FPGAs (synthesizable by Cadence-BuildGates, Synopsys Design Compiler, Synplify-Pro)
- Generated hardware optimized for datapath-synthesis tools (BG with datapath option and DC-Ultra)

- The design can be simulated in pure C or as a mix of C and generated HDL by using the Signal Processing Designer HDS option and the BER results can be verified.

Downlink STTD Channel

This reference system is the same as the Downlink Channel, except that it implements Space Time Transmit Diversity in the transmitter and receiver models. The system can be used to verify the DCH demodulation performance requirements in 3GPP TS 25.101 section 8.6.1.

Downlink Searcher

This reference system has the same transmitter and channel model as the Downlink Channel, but the receiver is replaced with a searcher. The searcher is a practical model that uses a matched filter to find and sort the strongest received signal paths. The searcher model can find up to six simultaneous signal paths.

Fast Cell Search

The Fast Cell Search reference system models the procedure a mobile must perform to synchronize itself with the basestation. The cell search is done in three phases. First the primary synchronization channel (PSCH) is used to obtain slot synchronization. Second, the secondary synchronization channel (SSCH) is used to obtain frame synchronization and to discern the code group for the basestation's scrambling code. Finally the scrambling code is selected from the 8 possible long codes in the long code group.

An interactive display shows the slot and frame offset, the code group and the selected scrambling code. The interactive display also allows the code group, code number and channel delay to be altered while the simulation is running to observe how quickly the fast cell search algorithm reacquires synchronization and the scrambling code number.

Basestation Model Details

- Primary and Secondary Synchronization Channels (SCH)
- Common Pilot Channel (CPICH)

- Primary Control Physical Channel (PCCPCH)
- Paging Indicator Channel (PICH)
- 16 channel Orthogonal Channel Noise Simulator (OCNS)
- Long and short scrambling code generation
- Dynamic runtime control of scrambling code group and number

Channel Model Details

- Static, fading cases 1 through 4, moving and birth-death channel conditions

Receiver Model Details

- Slot alignment through weighted multi-slot averaged matched filter output
- Group indicator codes (GIC) through weighted Hadamard transform peak detection
- Frame alignment and group code through table matched group indicator codes
- Scrambling code selection through short term correlation

Uplink Channel

The Uplink Channel reference system models single, high bandwidth data link from the user terminal to the base station. In its standard configuration the uplink reference system multiplexes two transport channels, DTCH and DCCH, onto a single physical channel for transmission. However just like the downlink the number of transport channels can easily be modified. The uplink uses two channel models to simulate a basestation using an ideal diversity receiver. The standard measurement channels 12.2kbps, 64kbps 144kbps and 384kbps can easily be simulated by using parameter presets. This reference system can be used to verify the DCH demodulation performance requirements in 3GPP TS 25.104 sections 8.2, 8.3, 8.4 and 8.5.

Transmitter Model Details

- Transport channel generation and coding
- Compressed mode with spreading factor reduction, higher layer scheduling modes
- Long and short scrambling code generation
- Transport format combination indicator coding
- Turbo and convolutional coding

- CRC generation
- Pilot symbol generation
- First and second interleaver
- Fixed and flexible frame positions
- OVFS code generation

Channel Model Details

- Static, fading cases 1 through 4, moving and birth-death channel conditions

Receiver Model Details

- Ideal diversity receiver model
- Compressed mode supported
- First and second deinterleaver
- CRC checking
- Transport format combination indicator decoding
- Turbo code scaling
- Viterbi decoder
- Turbo decoder supporting two different algorithms
- Rate de-matcher
- Block error rate and bit error rate is calculated

Uplink HSUPA

The Uplink HSUPA reference system models the E-DCH (Enhanced Dedicated Channel) and E-DPCCH (Enhanced Physical Control Channel) as described in 3GPP Release 6. It supports all UE Categories and is configured to run the performance requirements described in TS 25.104 section 8.11. The system includes transmitters for all Uplink channels and diversity receivers for E-DPDCH and E-DPCCH. The system configuration can easily be changed by disabling HS-DPCCH and/or DPDCH and turning off diversity. The E-DCH uses information from the E-DPCCH receiver for reception and decoding. The HARQ protocol is implemented and used to decode the E-DCH using incremental redundancy combining. After decoding the E-DCH data is verified through CRC and used to measure the data throughput. As part of the HARQ protocol an ACK or NACK is signaled to the transmitter data source.

- System includes E-DCH, E-DPCCH, HS-DPCCH, DPCCH and DPDCH uplink channels

- Simulation scripts covers 3GPP performance requirement tests in TS 25.104 section 8.11
- All Fixed Reference Channels, FRC1-FRC7, in TS 25.104 Annexes A.9 to A.11 parametrised
- E-DCH and E-DPCCH models support 2 or 10 ms TTI
- Included DPDCH and HS-DPCCH transmitter models can be turned on or off
- Receiver diversity can be enabled or disabled
- Compressed Mode supported in both 2 and 10 ms TTI mode
- HSUPA Category 6 UE:s with 5.76 Mbps max bitrate supported
- Hybrid-ARQ protocol with retransmissions and combining implemented
- E-DCH Turbo and E-DPCCH Reed-Muller encoding and decoding included
- E-DPDCH models support 1,2 or 4 physical channels
- E-DPDCH models supports spreading factors 256 to 2
- E-DPDCH IQ branch mapping using Nmax-dpdch and HS-DSCH configuration parameters
- E-DPCCH E-TFCI, Retransmission Sequence Number and happy fields implemented
- 3GPP Channel Model with five presets, Pedestrian A, Pedestrian B, Vehicular 30, Vehicular 120 or AWGN
- Selectable channel model oversampling rate (1x, 2x, 4x or 8x)
- Transmitter data source supports E-DCH frame retransmissions
- Data throughput collected and calculated
- ACK/NACK or DTX generated and signalled to transmitter with optional channel degeneration
- Models allow Transport Block Size, Redundancy Version, Spreading Factor and number of physical channels to change during simulation
- Ideal E-DCH and E-DPCCH diversity receiver models
- Uplink DPDCH transmitter supports dynamic multi-code

Uplink HSDPA

The Uplink HSDPA reference system models HS-DPCCH (High Speed Dedicated Physical Control Channel) that transmits feedback information for an associated HS-DSCH channel from the user terminal to the base station.

- HS-DPCCH implementation including CQI and HARQ-ACK
- Ideal HS-DPCCH diversity receiver model
- CQI encoding and decoding models
- HS-DPCCH mapping to I or Q branch is configurable
- Full downlink DPDCH and DPCCH coding and transmission included in system
- Uplink DPDCH transmitter supports dynamic multi-code
- Compressed Mode is supported

Uplink RACH Message Reception

The Random Access Channel Message Reception reference system consists of message frame generator, a transmitter, a channel model and an ideal receiver that measures the block error rate. The RACH message frames are convolutionally coded and a combined with a control frame consisting of pilot and TFCI symbols. The receiver model uses diversity to increase performance. The system supports all the test cases in the 3GPP TS 25.104 section 8.7.2 performance requirements.

Uplink RACH Preamble Detection

This verification system models the detection of transmitted RACH preamble sequences. The preamble sequences are generated and transmitted over the standard 3GPP channel model. A non-ideal diversity receiver uses matched filters to detect the sequence. Only a predetermined preamble signature can be detected. This system can be used to verify the RACH performance requirements in 3GPP TS 25.104 section 8.7.1.

The Signal Processing Designer TD-SCDMA Library

The Time Division — Synchronous CDMA (TD-SCDMA) library covers the Low Chip Rate (LCR) Time Division Duplex (TDD) of the

3GPP standard. The TD-SCDMA reference systems included in the library are as follows:

TD-SCDMA Downlink System

- Uses same channel encoder/decoder as 3GPP uplink system
- Uses same set TFC block as 3GPP downlink system
- Frame processing includes bit scrambling
- Second interleaver can operate over frames or timeslots
- Modulation using QPSK, 8-PSK or 16-QAM (only QPSK and 8-PSK used in normative channels)
- 1–16 Physical channels, all with the same spreading factor
- OVFSF channelization codes are phase shifted based on length and code number.
- Spread data is scrambled before inserting midamble
- Normative channels for 12.2, 64, 144, 384 and 2048 kbps

- 0–16 Channels of other users, DPCHo

TD-SCDMA Uplink System

- Uses same channel encoder/decoder as 3GPP uplink system
- Uses same set TFC block as 3GPP downlink system
- Frame processing includes bit scrambling
- Second interleaver can operate over frames or timeslots
- Modulation using QPSK, 8-PSK or 16-QAM (only QPSK used in normative channels)
- OVFSF channelization codes are phase shifted based on length and code number.
- Spread data is scrambled before inserting midamble
- 1 or 2 physical channels with different spreading factors
- Normative channels for 12.2, 64, 144, 384 kbps
- 0–8 Independent transmitters (other users), DPCHo.

Key Library Blocks**Partial list of downlink blocks**

- Compressed Mode Gain
- Downlink Common Channels
- Downlink Common Channels STTD
- Downlink Demodulation
- Downlink Frame Deformat
- Downlink Frame Format
- Downlink Frame Processing
- Downlink Ideal Receiver
- Downlink Ideal Receiver and Deformatting
- Downlink Ideal STTD Receiver and Deformatting
- Downlink Rate Match
- Downlink Scramble
- Downlink Scramble and Filter
- Downlink Single Code Spreading
- Downlink Single Code STTD Transmit
- Downlink Single Code Transmit
- Downlink Symbol Derepeat
- Downlink Symbol Repeat
- Downlink TrCH Decode
- Downlink TrCH Encode
- Downlink Turbo Scaling
- First Interleaver
- Hierarchical Golay Sequence
- OVSF Code Generator
- Paging Indicator Channel
- PN Sequence Generator
- Primary Common Control Physical Channel
- Primary Synchronization Channel
- Second Interleaver
- Secondary Synchronization Channel Downlink Searcher
- Secondary Synchronization Code Decoder
- STTD Encode
- STTD Frame Encode
- TFCI Decode
- TFCI Encode

Partial list of HSDPA blocks

- HARQ Combiner
- HARQ Interleaver
- HARQ Transport Block Source
- HSDPA Channel Coefficient Estimation
- HSDPA Rate Dematch Stage 1
- HSDPA Rate Dematch Stage 2
- HS-DSCH Rate Match
- HS-DSCH Bit Scramble
- HS-DSCH Constellation Rearrangement
- HS-DSCH CRC Check
- HS-DSCH Decoder
- HS-DSCH Demodulator
- HS-DSCH De-scrambler
- HS-DSCH Encoder
- HS-DSCH Interleaver
- HS-DSCH Modulator
- HS-DSCH Multicode Demodulator
- HS-DSCH Multicode Spreader
- HS-DSCH Receiver
- HS-DSCH Scrambler
- HS-DSCH Transmitter
- HS-SCCH CRC Check
- HS-SCCH Decoder
- HS-SCCH Demodulator
- HS-SCCH Encoder
- HS-SCCH Rate Match 1
- HS-SCCH Rate Match 2
- HS-SCCH Receiver
- HS-SCCH Spreader
- HS-SCCH Transmitter
- HS-SCCH UE Specific Demasking
- HS-SCCH UE Specific Masking
- Multicode Demodulator
- Multicode Slot Deformat
- Multicode Slot Format
- Multicode Spreading
- HS-DPCCH CQI decoder
- HS-DPCCH CQI encoder
- HS-DPCCH Receiver
- HS-DPCCH Transmitter

- Uplink DPCCH Frame Format
- Uplink DPDCH Frame Format

Partial list of HSUPA blocks

- HSUPA Data Source
 - HSUPA Redundancy Version Generator
 - E-DCH Encoder
 - E-DCH Interleaver and Deinterleaver
 - E-DCH Rate Dematch
 - E-DCH Rate Match
 - E-DCH TBS Calculation
 - E-DPCCH Decoder
 - E-DPCCH Encoder
 - E-DPCCH Receiver
 - E-DPCCH Transmitter
 - E-DPDCH Decoder
 - E-DPDCH Frame Deformat
 - E-DPDCH Frame Format
 - E-DPDCH Receiver
 - E-DPDCH Transmitter
 - HARQ Combiner
 - HSPA Data Throughput
 - Multi Channel Despreader
 - Single Channel Despreader
 - ACK/NACK/DTX Generator
- Partial list of uplink blocks**
- Uplink Demodulator
 - Uplink Frame Deformat
 - Uplink Frame Derepeat
 - Uplink Frame Format
 - Uplink Frame Processing
 - Uplink Gain Calculation
 - Uplink Ideal Receiver
 - Uplink Ideal Receiver and Deformat
 - Uplink Long Code Generator
 - Uplink Rate Match
 - Uplink Scramble and Filter
 - Uplink Scrambling Code
 - Uplink Single Code Spreading
 - Uplink Single Code Transmit
 - Uplink Symbol Derepeat
 - Uplink Symbol Repeat

- Uplink TrCH Decode
- Uplink TrCH Encode
- Uplink Turbo Scaling
- Partial list of RACH blocks**
- Pilot Generator
- Preamble Generator
- RACH Preamble Diversity Detector
- RACH Uplink Control Format
- RACH Uplink FFT Detector
- RACH Uplink Ideal STTD Receiver
- RACH Uplink Ideal STTD Receiver and Deformat
- RACH Uplink Preamble Detector
- RACH Uplink Transmit
- Partial list of practical receiver blocks**
- Comparator and Chip Adjustment
- Correlate and Dump
- Golay Sequence Match Filter
- Loop Filter
- Practical Rake Receiver and Slot Deformat
- Practical Rake Receiver Finger
- Partial list of practical receiver RTL blocks**
- Practical Rake Receiver Combiner
- Coherent Delay Locked loop
- Practical Rake Receiver Finger
- Pilot Power Estimation
- Downlink Scrambler-long Code Generator
- OVSF Code Gen-Short Code Generator
- Rake Signal Combiner
- DLL Control
- Rake Finger Control
- Pilot Power Control

Partial list of propagation model blocks

- 3GPP Channel
- Channel Delays
- Channel Weights and Filter
- Complex Gaussian Noise
- Compressed Mode Control Block
- OCNS Generator
- STTD OCNS Generator

Partial list of channel coding blocks

- Convolutional Encoder
- MAP Decoder
- Recursive Convolutional Encoder
- Turbo Decoder
- Turbo Demultiplex
- Turbo Interleaver
- Turbo Multiplex
- Vector CRC
- Viterbi Decoder
- Signal creation

The Signal Processing Designer WCDMA library offers the designer a faster way to market with improved opportunity for first-time success. The library enables a design team to quickly build complete system models including all the major systems of a network or personal communications device. Appropriate portions of the system model can be refined to generate RTL and the test-bench shared with other team members. As we move forward, CoWare will continue to track standards changes and offer the best libraries for your development efforts.

Customer Focus

CoWare provides a complete range of training, support, design methodology consulting, and integration services. Technical support requests are handled directly by experienced design engineers who are fully familiar with the application of CoWare tools and methodologies to real-world designs. Training courses are available at CoWare offices or at the customer site and can be tailored to meet the specific needs of the design team.

Sales Offices

CoWare has sales offices in the U.S., Europe, Asia Pacific and Japan. For a complete listing with contact information visit www.coware.com. For technical or sales information call 1-888-CoWare8 or email info@coware.com.



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